Experimental Validation of Common Mode Voltage Reduction PWM Algorithms in VSI fed AC Drive

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Abstract— *Modern day switching devices such as IGBTs have fast switching nature leading to increase in Common Mode voltage and its adverse effects. This paper presents reduced Common-Mode Voltage Pulse width modulation (RCMV-PWM) algorithms for the three-phase voltage source inverter driven Induction motor. PWM methods are reviewed and their pulse patterns and common mode voltage patterns illustrated. However, the Space Vector PWM (SVPWM) algorithm gives more Common Mode Voltage (CMV) variations due to the usage of zero voltage vectors. Moreover, the conventional SVPWM algorithm needs the angle and sector information for the calculation of switching times, which increases the complexity of PWM algorithm. In the proposed algorithm, active voltage vectors are used to program the output voltage using the concept of imaginary times. As the proposed method did not use sector identification and angle information, it reduces the complexity involved in conventional methods. In the proposed approach, by adding a unique zero sequence signal to the phase voltages, the modulating signals are derived. Then by comparing the modulating signals with triangular signals, the gating pulses for the various PWM algorithms are derived. As the proposed PWM algorithms did not use the zero states, these results in reduced CMV variations. To validate the proposed algorithms, several numerical simulation studies and Experimental tests have been carried out on v/f controlled induction motor drive.*

Keywords— **Common Mode Voltage, SVPWM, Scalar approach, AZSPWM.**

I. INTRODUCTION

In the most of industries like oil sector, gas sectors, In the past DC motors were widely preferred since control of a DC motor is easy and its speed can be Controlled by changing its Terminal voltage. However, they have disadvantages against AC induction motors such as their initial and maintenance costs. AC motors are economical but it is impossible to control an AC motor efficiently by directly feeding it from the AC grid. Therefore, Adjustable Speed Drives (ASD) were developed. Nowadays the adjustable speed induction motor drives becoming very popular in many industrial applications due to their rugged construction and reliable operation. Three-phase Voltage Source Inverters (VSIs) are widely utilized to drive AC motors with high motion control quality and energy efficiency. Hence in order to obtain the controllable supply from the inverter, recently the PWM algorithms are introduced. However, there is a large load star point to the center of the dc- bus of the VSI (Vno in Fig.1) potential and can be expressed as [6] variety of PWM methods that exhibit unique performance characteristics and the choice and utilization of a specific PWM method among many is not a simple task. A detailed survey on various PWM algorithms is studied in [1]. PWM mostly involves the standard Continuous PWM (CPWM) methods such as the Sinusoidal PWM (SPWM) and Space Vector PWM (SVPWM), and the Discontinuous PWM (DPWM) methods. However, the performance characteristics of the recently developed Reduced Common Mode Voltage PWM (RCMV-PWM) methods are also studied [2].

In the standard three-phase two-level Voltage Source Inverter (VSI) with diode rectifier front-end, which is shown in fig.1. The CMV is defined as the potential of the star point of the load with respect to the power line ground (Vng) which is expressed as Vng = (Vno + Vog). Since Vog being much smaller and slowly varying signal compared to Vno, the V og term can be neglected. Therefore, the CMV of the inverter is equal to Vng = Vno. The inverter pole voltages are given by,

$$V_{ao} = V_{an} + V_{no} \quad (1)$$
$$V_{bo} = V_{bn} + V_{no} \quad (2)$$
$$V_{co} = V_{cn} + V_{no} \quad (3)$$

By adding above three equations since, the instantaneous phase voltages are zero i.e. Van +Vbn + Vcn = 0. Then the above equation reduces to Vno = Vng = (Vao + Vbo +Vco)/3. (4)

When the induction motor is fed from a 3-phase balanced supply, the CMV is zero. Since the VSI cannot provide sinusoidal voltages and has discrete output voltages synthesized from fixed dc-bus voltage Vdc, always VSI exhibits the CMV variations. The amplitude of the CMV is always different from zero and may take the values of ±Vdc/6 or ±Vdc/2, will depend on the inverter switching states selected. All conventional CPWM and DPWM methods exhibit high CMV characteristics that pose problems in the application field. At switching frequencies above several kilohertz, excessive CMV with sharp edges can result in high Common Mode Currents (CMC). In motor drive applications, this may lead to motor bearing failures, electromagnetic interference noise that causes nuisance trip of the inverter drive, or interference with other electronic equipment in the vicinity. In the application field, such problems have increased recently due to increasing PWM frequencies and faster switching time and CMV reduction techniques have gained importance. Passive or active filters can be utilized to suppress the effect of the CMV of two-level inverter [7]. Also, a three-level inverter could be employed to decrease the CMV from the source [7]. However, all these methods involve external/additional hardware, and thus, they significantly increase the drive cost and complexity. An alternative approach is to modify the PWM pulse pattern of the classical two-level inverter. Hence, nowadays, many researchers focused their interest on the development of various PWM algorithms [2] for the CMV effects to mitigated at no cost. In the survey, various PWM pulse-pattern-modification based CMV reduction methods have been reported. To be classified as reduced CMV PWM (RCMV-PWM) methods such as Active-Zero State PWM (AZSPWM), Remote-state PWM (RSPWM), near state PWM (NSPWM) these are the most successful representatives. In all these methods the maximum CMV is reduced from ±Vdc/2 of the conventional PWM methods to ±Vdc/6, and also with this type PWM switching the switching loss also reduced. But while in conventional CPWM such as SPWM, SVPWM, and DPWM are the methods with maximum CMV varies between ±Vdc/2 to ±Vdc/6 these variations are due to the usage of zero voltage vectors. Therefore, it is necessary to eliminate usage of zero voltage vectors this is achieved in RCMV-PWM methods [4].

II. CONVENTIONAL SVPWM ALGORITHM

The converters which produce an output voltage or current with level either zero or +Vdc /-Vdc are known as two level converters. In high power and high voltage applications this two level inverter however have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating. In 2-level inverter output voltage waveform is produced by using PWM with two voltage levels, this causes the output voltage and current to be distorted and the THD of the voltage is poor. Figure 1 shows the schematic circuit diagram of two level inverter.

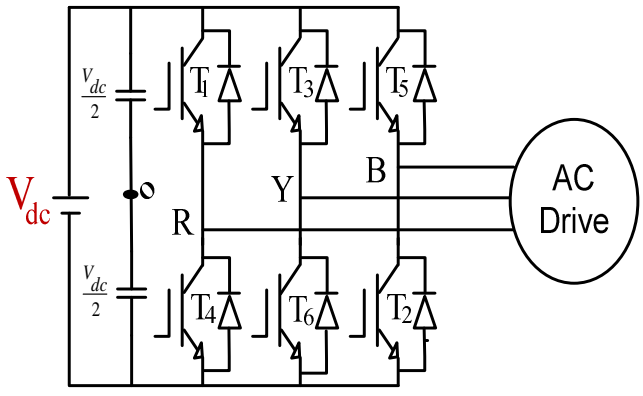


Figure1. Three Phase Voltage Source inverter schematic diagram

The Space Vector Pulse Width Modulation (SVPWM) refers to a special switching sequence of the upper three power devices of a three-phase voltage source inverters (VSI) used in application such as AC induction motor drives.

It is a more sophisticated technique for generating sine wave that provides a higher voltage to the motor. Space Vector PWM (SVPWM) method is an advanced; computation technique intensive PWM method and possibly the best techniques for variable frequency drive application. In SVPWM technique, where the complex reference voltage vector is processed as a whol. The space vector PWM is realized based on the following steps

The reference voltage vector (Vref) is sampled at equal intervals of time, Ts referred to as sampling time period. Different voltage vectors that can be produced by the inverter are applied over different time durations with in a sampling time period such that the average vector produced over the sampling time period is equal to the sampled value of the Vref, both in terms of magnitude and angle. It has been established that the vectors to be used to generate any sample are the zero voltage vectors and the two active voltage vectors forming the boundary of the sector in which the sample lies. As all six sectors are symmetrical for the required reference voltage vector, the active and zero voltage vectors times can be calculated as in (5), (6) and (7).

$$T1 = (2\sqrt{3}/\pi)*Mi*\sin(60^{o} - \alpha)*Ts \quad (5)$$
$$T2=(2\sqrt{3}/\pi)*Mi*\sin(\alpha)*Ts \quad (6)$$
$$Tz = Ts - (T1+T2) \quad (7)$$

Where Mi is the modulation index and Tz total zero voltage vector time equally divided between Vo and V7 and distributed symmetrically at the start and end of each sampling time period. Thus, SVPWM uses 0127-7210 in Sector-I, 0327-7230 in sector-II and so on [5]. Since SVPWM algorithm needs the angle and sector information for the calculation of switching times, which increases the complexity of PWM algorithm. Hence, to reduce the complexity involved in the PWM and CMV variations various PWM algorithms have been developed using the concept of imaginary switching times of carrier based scalar approach.

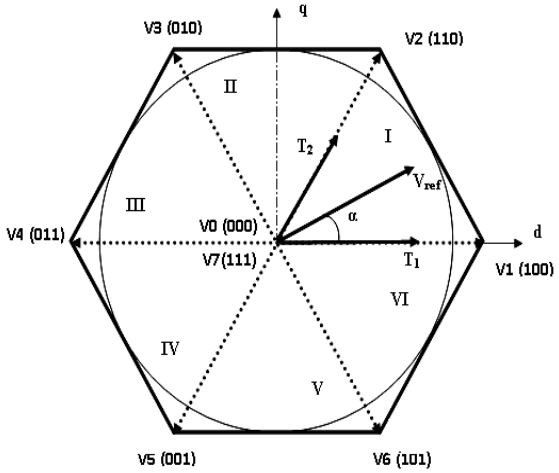


Figure 2: SVPWM switching vectors and sectors selection

From TABLE.1, it can be concluded that the CMV may take the values ±Vdc/6 for the active states and ±Vdc/2 for zero states. Hence for the reduction of CMV, the zero states should be avoided.

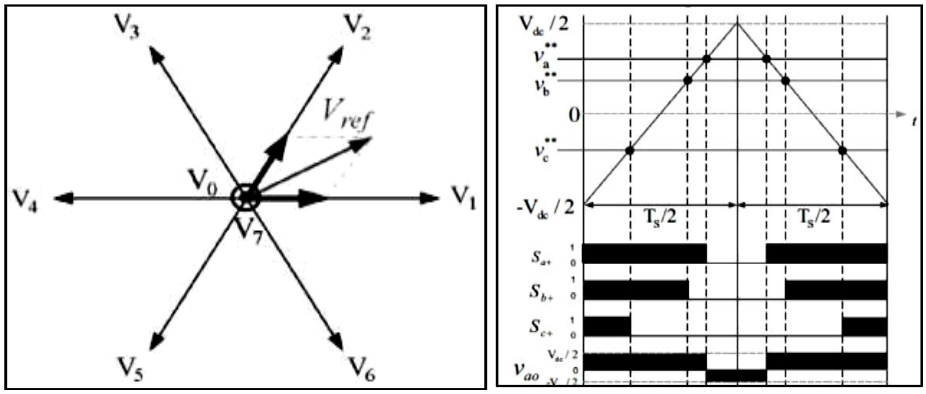
Table 1: Pole Voltage and CMV Generated for Various Switching States

Switching states	Inverter Pole Voltages			Vng= Vno (CMV)
	Vao	Vbo	Vco	
Vo (000)	-Vdc/2	-Vdc/2	-Vdc/2	-Vdc/2
V1(100)	Vdc/2	-Vdc/2	-Vdc/2	-Vdc/6
V2(110)	Vdc/2	Vdc/2	-Vdc/2	Vdc/6

V3(010)	-Vdc/2	Vdc/2	-Vdc/2	-Vdc/6
V4(011)	-Vdc/2	Vdc/2	Vdc/2	Vdc/6
V5(001)	-Vdc/2	-Vdc/2	Vdc/2	-Vdc/6
V6(101)	Vdc/2	-Vdc/2	Vdc/2	Vdc/6
V7(111)	Vdc/2	Vdc/2	Vdc/2	Vdc/2

III. CMV PATTERNS FOR SVPWM AND AZSVPWM METHODS

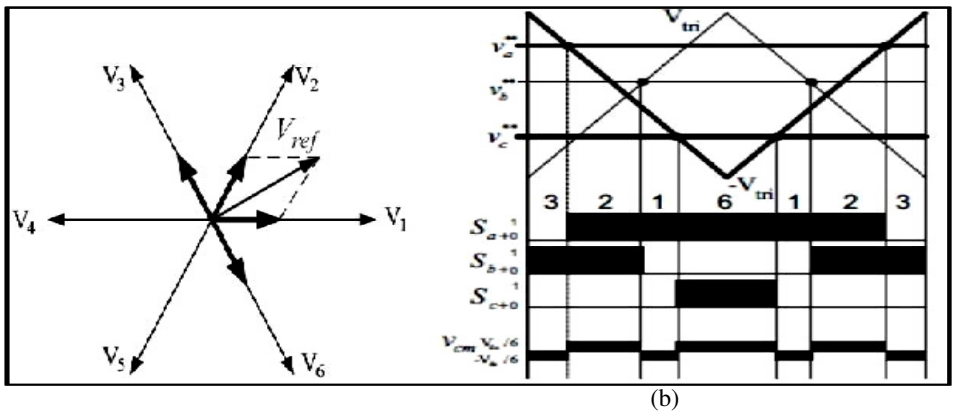
Based on the modulation signal, conventional PWM methods are classified as the Continuous PWM (CPWM) (SPWM, SVPWM) method and the DPWM (DPWM1,2, etc.) method. The pulse pattern of the CPWM and DPWM methods involves utilization of at least one of zero voltage vector V0 and V7 during each PWM cycle. The switch pulse pattern of the SVPWM method (t0=t7) is shown in Fig. 3(a) in such patterns i.e.., (CPWM and DPWM methods) yield high common mode voltage (±Vdc/2). Hence, several PWM pulse patterns that yield reduced common mode voltage have been reported. These, and several low common mode voltage methods reported in this approach will all be grouped under the name of RCMV-PWM methods. In SVPWM utilize two active vectors adjacent to the reference voltage vector and the two zero vectors with equal time duration (t0=t7) in each PWM cycle.



(b)

Figure 3: (a) voltage space vectors, and (b) SVPWM modulating signals, switch logic, phase and Line-line voltage and CMV pulse pattern

In AZSVPWM utilize the same active vectors as in SVPWM. However, instead of the real zero voltage vectors (V0 and V7), two active opposite voltage vectors with equal time duration are utilized to create an effective zero vector. For example, in A1 region, the V3-V6 pair is utilized since these vectors are adjacent to the V1-V2 vectors [3]. The pulse patterns and the resulting CMV for the specific regions of the voltage vector space is shown above. As absorbed from the figure, in these RCM-PWM methods, the inverter zero states are avoided and resulting in low CMV (±Vdc/6).



(b)

Figure 4: (a) voltage space vectors, and (b) AZSVPWM pulse pattern and CMV pattern

The utilized voltage vectors and their sequences for the conventional and RCMV-PWM methods are given below in [2] Table II.

Table 2: Region-Dependent Vector Patterns of Various PWM Methods

SVPWM	A1	A2	A3	A4	A5	A6
	7210-0127	7230-0327	7430-0347	7450-0547	7650-0567	7610-0167
AZSVPWM	A1	A2	A3	A4	A5	A6
	3216-6123	4321-1234	5432-2345	6543-3456	1654-4561	2165-5612

IV. RESULTS AND DISCUSSION

To validate the proposed work, simulation studies and experimental tests have been carried by using MATLAB/dSPACE. The switching frequency considered for simulation is 3 kHz and for hardware 1 kHz, the ratings of the induction motor considered as 3-pahse 50 Hz, 4-pole, 1470rpm, 4 kW with the following parameters.

Rs= 1.57Ω, Rr = 1.21Ω, Ls = 0.17H, L r = 0.17H,

Lm = 0.165 H and J = 0.089 Kg.m^2.

A) Simulation Results:

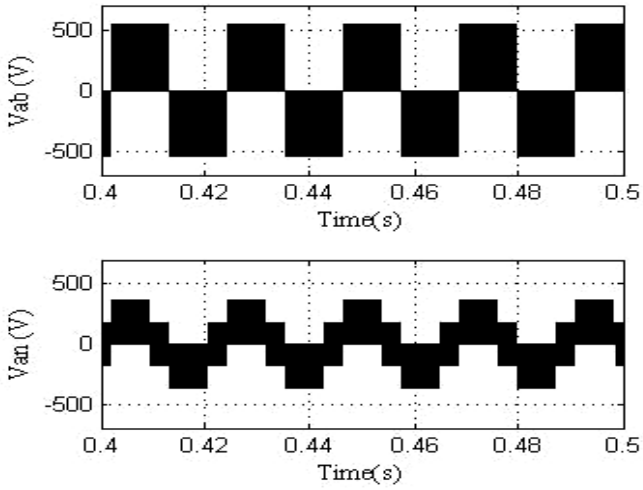


Figure 5: Phase voltage and Line voltage: SVPWM

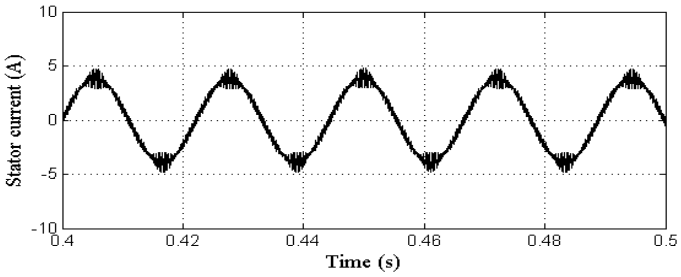


Figure 6: Stator current: SVPWM

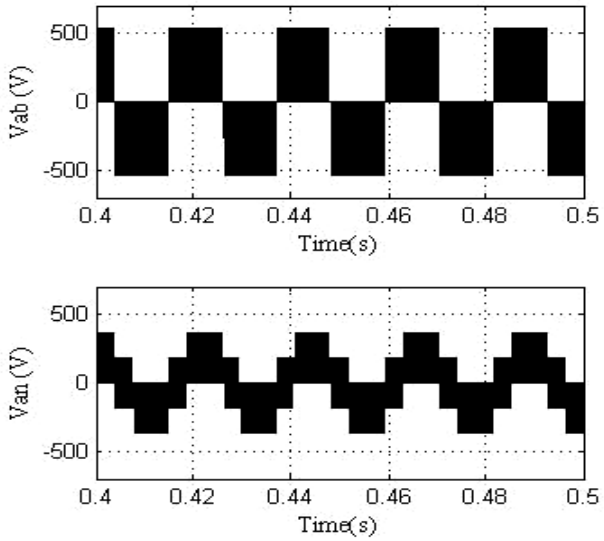


Figure 7: phase voltage and Line voltage: AZSVPWM

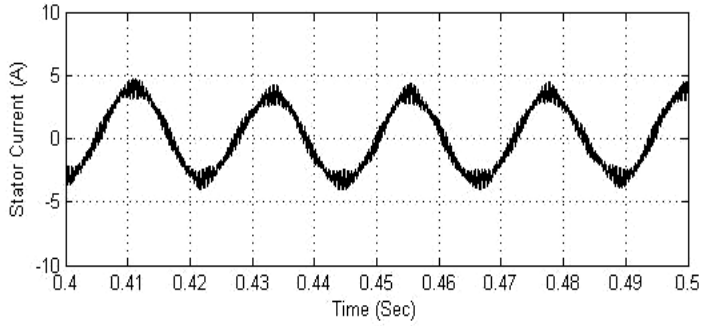


Figure 8: Stator current: AZSVPWM

B) Hardware Results:

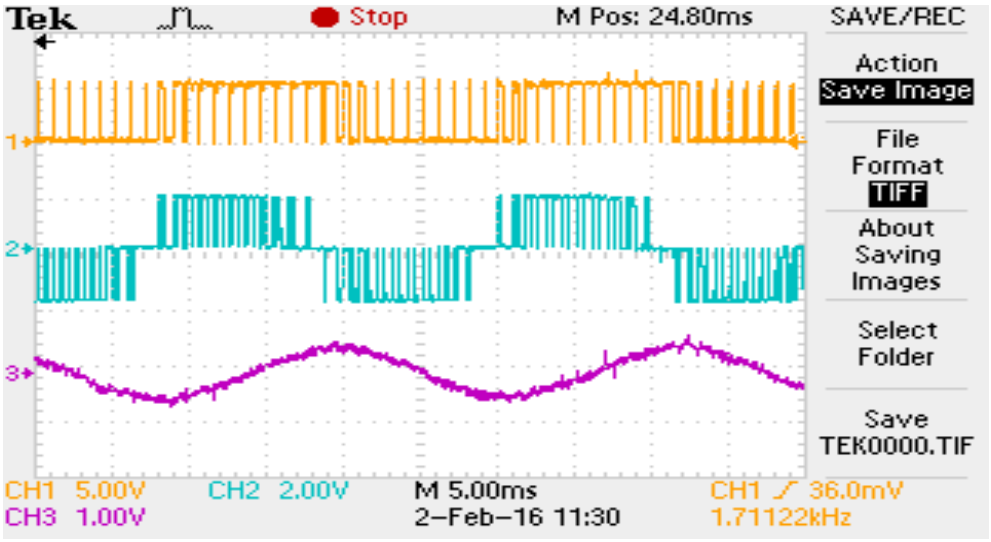


Figure 9: Pole Voltage, Line voltage and stator current: SVPWM

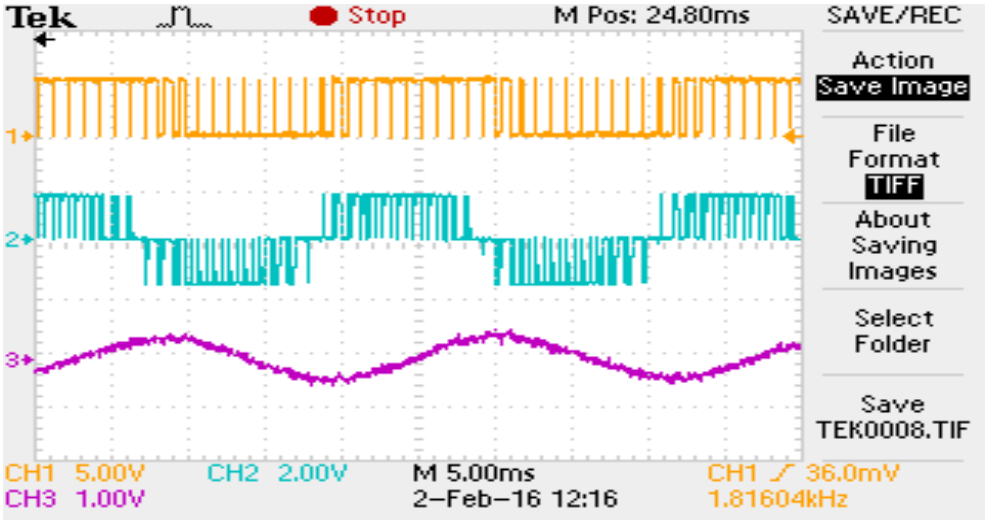


Figure 10: Pole Voltage, Line voltage and stator current: AZSVPWM

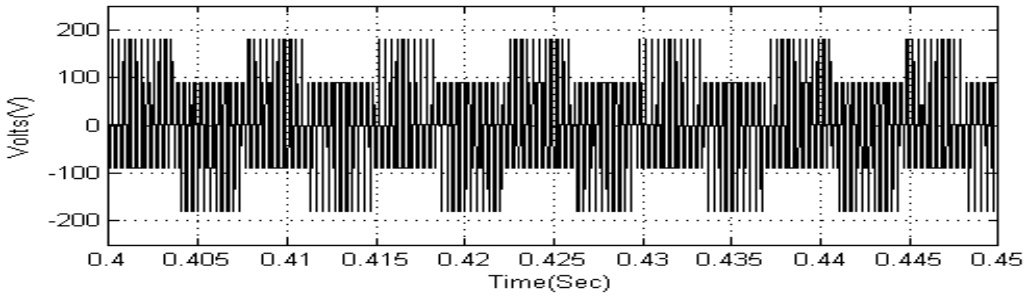


Figure 11: Common mode voltage: SVPWM (Simulation)

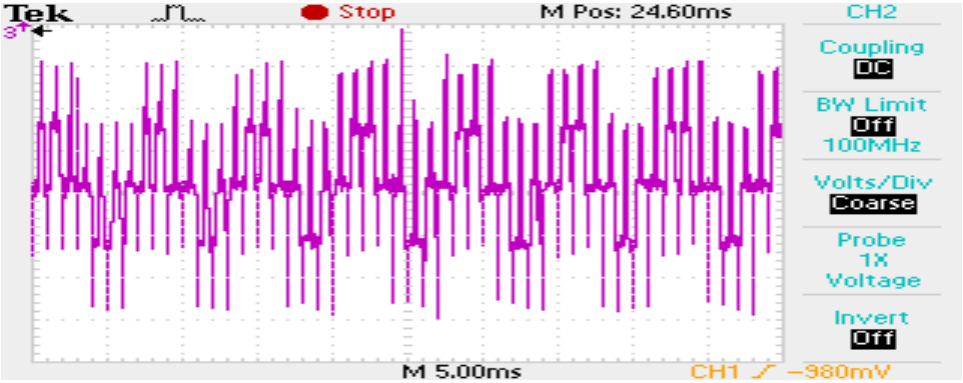


Figure 12: Common mode voltage: SVPWM (Hardware)

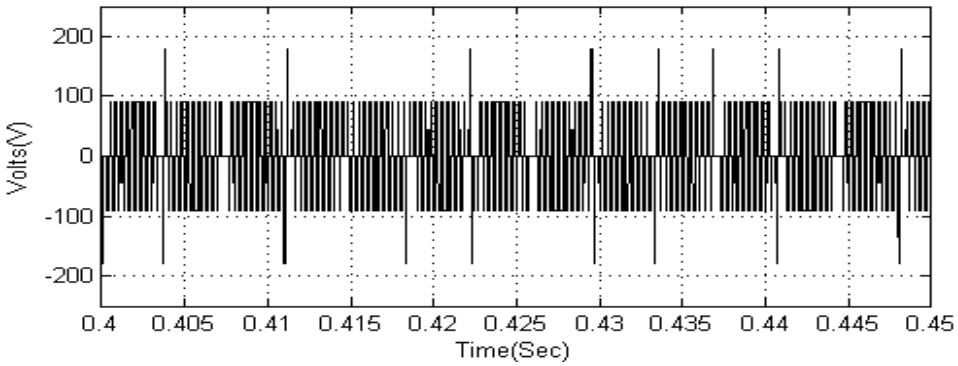


Figure 13: Common mode voltage: AZSVPWM (Simulation)

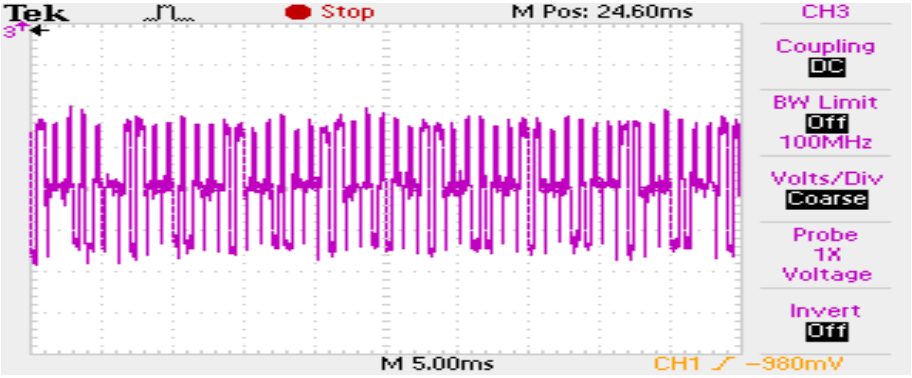


Figure 14: Common mode voltage: AZSVPWM (Hardware)

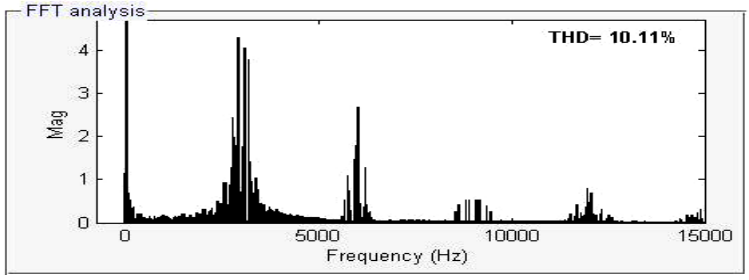


Figure 15: harmonic spectrum of stator current: SVPWM

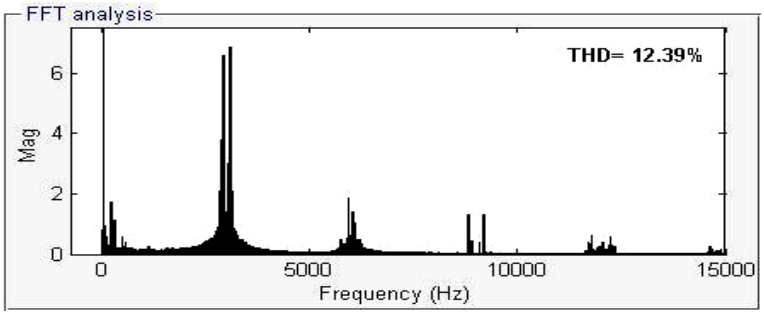


Figure 16: harmonic spectrum of stator current: AZSVPWM

Table 3: Performance Comparison of Proposed PWM Methods

PWM	THD	CMV
SVPWM	10.18%	Vdc/2
AZSPWM	15.26%	Vdc/6

V. CONCLUSIONS

In an inverter-driven AC machine, the common-mode voltage and dv/dt may cause premature motor bearing failure. This paper compared the SVPWM and reduced common mode voltage PWM algorithm for VSI fed induction motor drive. From the results it can be observed that the SVPWM gives large common mode voltage variations between ±Vdc/2. But, the proposed AZSVPWM algorithm gives the reduced CMV variations between ±Vdc/6. Moreover, it can be observed that the proposed AZSVPWM algorithm give opposite pulses in line to line voltages, which causes the increased harmonic distortion in the line current.

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