A Power Efficient Flip Flop by using 90nm Technology

Mrs. Y. Lavanya
Associate Professor, ECE Department,
Ramachandra College of Engineering, Eluru,
W.G (Dt.), A.P, India.
Email: lavanya.rcee@gmail.com

Abstract- *In this paper, a power efficient flip-flop by using 90nm technology has been proposed in which two techniques are added to the existing system. The foremost one is to reduce the complexity and extra-switching. This is done by modifying the inverter and pass transistor to the pulse generator circuit. The later one is to speed up the charging and discharging along the critical path only when it is needed. This is done by modifying the signal feed through technique. As a result of these techniques number of transistors has been reduced in the pulse generator circuit which in turn reduces in pulse generator circuit which in turn reduces the power and area required. The simulation results shown are based on the 90nm technology that compares different parameters.*

Keywords - **power-delay product (PDP), Flip-Flop (FF), pulse triggered, low power, Signal Feed Through (SFT), Conditional Pulse Enhancement (CPE), FF with minimum transistors.**

I. INTRODUCTION

At present scenario, high speed, low area and low powered devices plays a major role in designing a digital system. So, to meet the above mentioned demands, the flip flops are extensively used as basic storage elements in the digital systems which are faster and low powered. Now-a-days, the digital systems in VLSI, were often follow pipelining techniques and utilizes modules with many flip flops. Due to this, the power consumption of clock (CLK) system is as high as 25% to 48% of power consumption of the total system [1], where the clock system consists of distribution networks and storage elements. Hence, in high speed applications, pulse triggered flip flops (PT-FF) has been considered as a popular alternative to the established master-slave based flip-flop design. PTFF are also more rigid to clock jitter. Irrespective of these advantages, pulse generation circuitry requires gentle pulse width control in the shape of clock pulse distribution network and in the process variation. PTFF can be classified into 2 types namely, an explicit and an implicit PTFFs, based on the pulse generation method. In explicit type, the pulse generator circuit and the latch are separated whereas in implicit type, the latch design consists of a pulse generator as a built- in logic [2]. Long discharging path in latch design which leads to delayed timing characteristics is involved in implicit type design. The situation gets worse further when low-power techniques such as conditional precharge, conditional discharge conditional capture, or conditional data mapping are applied [3]. As a result, the transistors of pulse generation logic are often distended to confirm that the generated pulses are sufficiently wider to generate the data catching of the latch design. A similar type of pulse width control problem is also arose in Explicit PTFF. This problem is particularized in the presence of a large load capacitance, whenever one pulse generator is shared among several latches. By using proper clock pulse generator with proper sizing and switching activities the above problem can be solved. The circuit power dissipation depends on the parameters like clock frequency, power supply, load capacitance, transistor sizing and switching activities etc. The power dissipation will be more if these parameter values are high. So, it is necessary to choose ideal parameter values and better transistor sizing to make the system design more efficient in terms of power and speed [4].

In this paper, a power efficient FF by using 90nm Technology has been proposed along with some conventional developed FFs design that are shown in the Section II. Section III represents the proposed FF design with its operation. Section IV contains the simulation results and Section V gives the conclusion of this paper.

II. CONVENTIONAL DEVELOPED FFs DESIGN

There are numerous varieties of Flip-Flops which have been implemented as a Data (D) FF with 2 different techniques. In this paper, we have selected few best low powered FFs as references for the purpose of comparison. They are (i) Conditional Pulse Enhancement Pulse Triggered FF (CPEPT-FF) and (ii) Signal feed through FF (SFT-FF). The first one has the advantages of low power consumption and reduced leakage power whereas the second has the advantages of the power efficient and faster operation. Now the sections A and B gives the brief description on both techniques with the help of circuits. Fig. 1 shows CPEPT-FF [1] design. And Fig. 2 shows SFT-FF [2] design.

A) *Conditional Pulse Enhancement Pulse Triggered FF (CPEPT-FF)*

Fig. 1 below shows the design of CPEPT-FF [1]. Formerly, AND gate logic is used as NAND plus NOT gate to generate the clock pulse (CP) explicitly at the rising edge of the CLK. But CPEPT- FF technique uses a pass transistor based AND gate logic which reduces the no. of transistors required, CLK to CP delay. This makes the circuit faster and also low powered. An extra PMOS (P3) transistor is used at the top in parallel with PMOS (P2) transistor where node X acts as input. This node X enhances the CP height and width to switch ON the NMOS (N6) transistor properly, especially for the case when the longest discharging path occur due to input Data=1 and Qb=1. It is to be remembered that, this CPEPT-FF technique takes effects only when FF output is subjected to a data change from 0 to 1 (or) low to high transition. This leads to low power consumption in the FF circuit and also reduces the leakage power due to less no. of transistors in the discharging path. But, the main draw back in this technique is that the PMOS (P1) transistor is permanently grounded which increases some power dissipation when the switching of node X occurs.

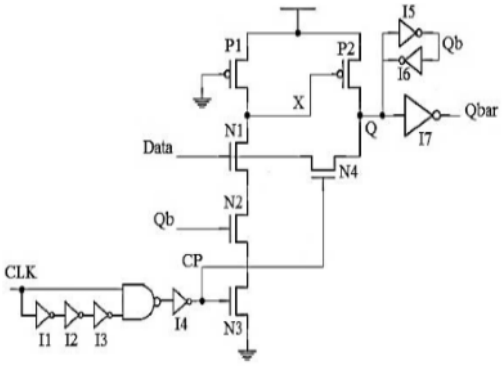

Fig. 1 Conditional pulse enhancement pulse triggered flip-flop (CPEPT-FF)

B. *Signal feed through FF (SFT-FF)*

Fig. 2 below shows SFT-FF [2] design. Signal feed through technique is the power efficient and faster operation technique which plays a significant role in charging and discharging of the output node Q. This circuit employs a static latch structure and the conditional discharge scheme to remove unnecessary switching at the internal and external nodes. Here, charging of node Q depends on PMOS (P2) transistor. But NMOS (N4) transistor is equally responsible for charging of Q when CP occurs at the rising edge of the CLK. When the Data input is at logic "1", Qb which is input to the NMOS (N2) is also at logic "1". When both are at logic '1', CP which acts as input to the NMOS (N4) transistor also occurs and then node X discharges through N1, N2 and N3 to ground and this switches ON the PMOS (P2) transistor. This will start node Q to charge but at the same time, transistor N4 is also ON due to occurrence of CP. So, Q charges rapidly through P2 and N4 transistors. Now N4 transistor is only responsible for the output node Q to discharge when Data becomes "0" and CP occurs. As this technique reduces the rise time and fall time for the charging and discharging of node Q, it is considered as a faster design. As we have seen the drawback in the first technique, the transistor P1 is responsible for a static leakage current that flows through transistor which increases the overall power dissipation in the circuit. The same problem was arose even in second one also. In addition to that, this technique also finds the problem of large area required. The clock pulse generation circuit of SFT-FF technique has more number of transistors, this increases area of the FF. Therefore, to overcome the drawbacks of large area required and large power dissipation, a modified design has been proposed in which it provides power efficient FF that reduces area required and power dissipation.

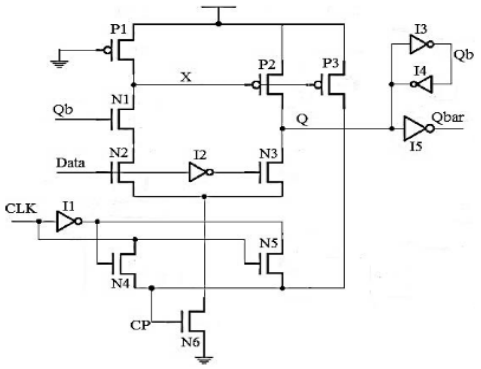

Fig 2 SFT-FF design

III. PROPOSED FF DESIGN

Fig. 3 shows the block diagram of proposed power efficient FF design which consists of the following blocks. They are (i) Serial Clock Pulse Generator, which consists of 3 NMOS transistors and 1 PMOS transistor. The two NMOS transistors are connected in series with PMOS and another NMOS is connected parallel to the PMOS. The output of CLK pulse generator is nothing but a clock pulse (CP). (ii)Pass Transistor, it is nothing but a combination of the 3 NMOS transistors. The output of the serial CLK pulse generated is connected with the pass transistor. The input for the three individual NMOS all Data, Qb, CP respectively. (iii) PMOS transistor, in which the first transistor of NMOS in the pass transistor is connected with the PMOS again. The input for the PMOS is CP which is nothing but a clock pulse. Here, we are using another PMOS. There is an interconnection between the pass transistor and PMOS and is termed as one node 'X'. (iv) NMOS transistor, in which there is a series combination of the PMOS and NMOS transistors again. (v) Signal Feed through Technique is nothing but the interconnection of two inverters. The output of the one inverter is connected as input to the second inverter. Finally, the output Qb is generated. Actually inverters are used to invert the given output, but here the inverter are used for the delay of the signal due to this delay the power consumption in the circuit decreases. But here we are using modified inverter in the proposed system to make the system power efficient.

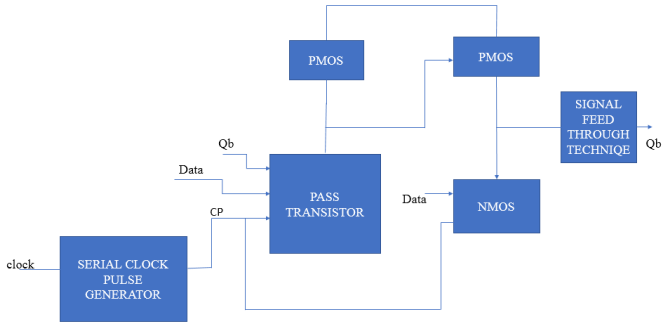

Fig. 3 Block diagram of proposed power efficient FF design

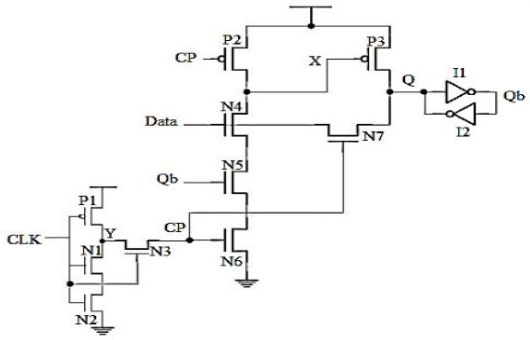

Fig. 4 Circuit diagram of Proposed FF design

Fig. 4 represents the circuit diagram of proposed power efficient FF design which has the minimum no. of transistors. This is designed in such a way that it contains only 4 transistors where all are connected to the CLK signal to generate CP at the rising edge of the CLK. In general, inverters are used to generate some delay in any signal. For reducing the power consumption, the inverter circuit is modified in the proposed method. When CLK is "0", then transistor N1, N2 and N3 are OFF but node Y is charged through transistor P1. When CLK changes from "0" to "1" or the rising edge of the CLK occurs, then transistor N3 is rapidly switched ON than transistor N1 and N2 due to its large size. So, node CP starts to charge till logic "1" but after sometime, node Y discharges through transistors N1 and N2 slowly due to their minimum size (length=width). It makes CP to drop to "0". But a pulse is generated due to the delay provided by two NMOS transistors in series. This CP is connected to three transistors P2, N6 and N7. When CLK is "0", then CP is also "0". So, transistor P2 is ON and node X charges. Here, we assume that node Q is previously "0" that makes Qb=1. If Data is also "1", then at the rising edge of the CLK signal, CP switched ON the NMOS transistor N6 and node X starts discharging. It makes transistor P3 ON and node Q starts charging. But at the same time, N7 is also switched ON which also helps to charge node Q through input Data. And CP makes P2 OFF at the discharging time of node X. So it dissipates less power during switching. When Data becomes "0" then at the occurrence of CP, output node Q is rapidly discharged to input data through N7. This signal feed through technique doesn't affect the input data source because N7 is switched ON only for few Pico seconds. Here we are using bi-stable principle, where the inverters I1andI2 are used to get inverted and stable output. As this design containing only 14 number of transistors which results in low power dissipation.

IV. SIMULATION RESULTS

In this paper, it has been shown that the 3 best low powered FFs in which one is proposed FF and the other two are conventional designs that are explained in section II and III. Here optimal results are obtained by using different techniques based FFs. By using CMOS 90nm process technology is used in this FFs. This makes it applicable in sub-

micron technology applications. Simulation results are obtained at 500 MHz CLK frequency and 1V power supply that makes this design suitable for low power applications. In high fan-out applications, a load capacitance of 20 fF is used at the output. Proposed FF has minimum Data-to Q delay that is 85.51 ps. Fig. 5 shows the simulation results of the proposed design FF, in which it shows the waveforms of CLK signal, Invertor output and Trigger output respectively.

Table I. shows the comparison of various FF designs performance and power dissipation at different switching activities. All results are optimized for the minimum PDP. Fig. 7 represents the graph of power-delay product (PDP) comparison of proposed FF with conventional FFs design.

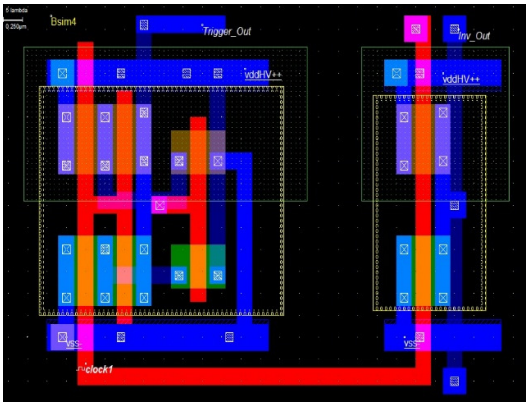

Fig. 5. Simulation Waveform of Proposed FF

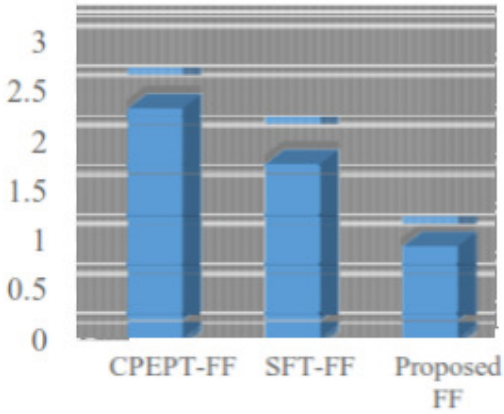

Fig. 6 Layout diagram of Proposed FF

Fig. 6 represents the layout diagram of the proposed power efficient FF design in which the MICROWIND software is used to draw the layout diagram of the proposed FF design. In order to draw this layout diagram, the MICROWIND display window has been used, which consists of the layout display window, the icon menu and the layer palette. The design procedure has been explained that the cursor appears in the middle of the layout window and is controlled by using the mouse. The layout window features a grid that represents the current scale of the drawing, scaled in lambda units and in micron. The lambda unit is fixed to half of the minimum available lithography of the technology. The default technology is a 0.8 µm technology, consequently lambda is 0.4 µm.

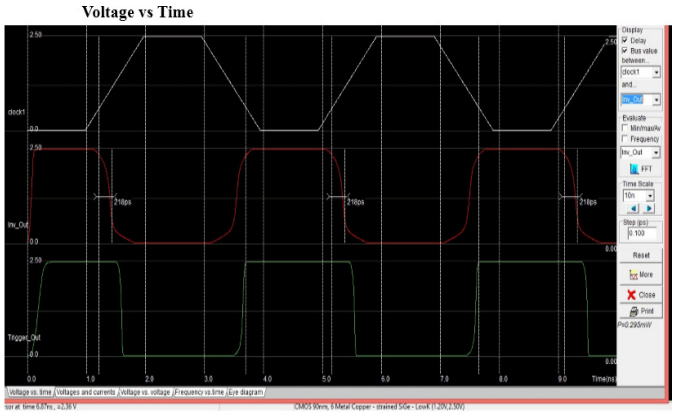

Fig 7. Comparison of PDP (fJ) at 50% switching activity with various FFs

Table 1. Comparison of Various FF Designs

Parameters/ Types of Flip –Flops in comparison	CPEPT-FF	SFT-FF	Proposed FF
No. of transistors	19	24	14
No. of Transistors in CLK pulse generator circuit	5	12	4
CLK tree power (uW)	7.72	8.13	3.79
Minimum Data-to-Q delay (ps)	117.56	103.21	85.51
Average Power (100% switching activity) uW	25.38	22.13	15.98
Average Power (50% switching activity) uW	20.55	18.01	12.02
Average Power (25% switching activity) uW	15.73	14.67	8.35
Average Power (0% all-1) uW	6.58	9.45	7.41
Average Power (0% all-0) uW	5.72	5.97	4.19
PDP (fJ) at 50% switching	2.41	1.85	1.02

V. CONCLUSION

A new power efficient using 90nm technology has been proposed. In this, the no. of transistors used had been reduced compared to the existing methods. Hence this reduces the area and power required. The results shows that proposed FF has lowest power at different switching activities and lowest Data-to-Q delay as compared to the existing methods. So, the proposed FF has lowest power delay profile (i.e., PDP= 1.02 fJ) as compared to other FFs PDP which is as shown in Table I. All these advantages of proposed FF make it applicable for the low powered and high frequency applications.

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BIOGRAPHY

Mrs. Y. Lavanya completed her B.Tech from Kuppam Engineering College, Kuppam in the year 2007 and completed M.Tech from St.Ann's College of Engineering & Technology, Chirala in the year 2013. At present, she is working as Associate Professor in ECE Department in Ramachandra College of Engineering, Eluru. She has 8 years of excellent teaching experience and published several research papers in various international journals and conferences.