DESIGN OF OPTIMIZED QCA SEQUENTIAL CIRCUITS

P.Azhagu Pradeepa[#1], G.Bamila Juliet[#1],G.Gogula Priya[#1] ,S.Karthigai Lakshmi[*2]
[#1]Student &*Department of Electronics and Communication&Anna University*
SSM Institute of Engineering and Technology,Tamilnadu,India.
[*2]Professor& *Department of Electronics and Communication&Anna University*
SSM Institute of Engineering and Technology,Tamilnadu,India.

***Abstract*- The scenario of the digital industry has changed in the past few years due to the rapid development of technology. Among several other alternatives, QCA is the innovative technology to design digital logic circuits using quantum dots confined in the potential well. This paper proposes the optimum design of sequential circuits like flip-flops and counters by using majority gates and is implemented by cell minimization technique. It will reduce the area and complexity. The functionality of the circuits can be tested by using QCADesigner version 2.0.3.**

Keywords- Quantum-dot cellular automata , sequential circuit, flip-flops, counters, QCADesigner.

I.INTRODUTION

To making the small transistor, it is a great advancement in electronics and computer industry over the past 60 years. In CMOS the serious effects due to physical barriers such as short channel effect, leakage current and excessive power dissipation at Nanoscale regions. Hence one possible alternative method is QCA to overcome this problem.QCA technology transfer's information by means of polarization using the flow of electrical current. It provides ultra-small factor, power consumption and high speed clock circuits.

A sequential circuit is a type of digital circuit who's the output depends on the present value of the input signal as well as the sequence of past inputs.

Types of sequential circuit:

1. Synchronous circuit: It uses the clock input to derive the circuit.
2. Asynchronous circuit: It doesn't use the clock signal to drive the circuit.

QCA is the new paradigm that performs computation and routing information at Nano domain. The advantage of QCA over the CMOS is lesser delay, high density circuit and low power consumption.

II.REVIEW OF QCA

The logic states are the unique feature of the QCA and it is represented by a cell. QCA cell contain four quantum dots arranged in corners of the square. Then two electrons are used to provide a tunneling between these two dots. The polarized charge can transfer by the columbic repulsion within the square cells.

A basic QCA cell consists of four quantum dots in square array.

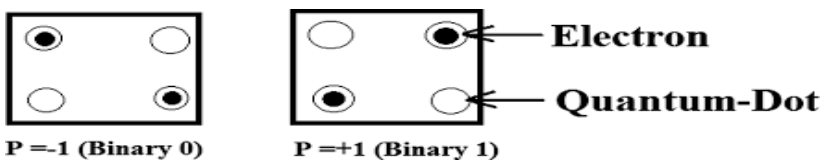

Fig.1 Polaraized QCA cells

Polarization p=-1and p=+1 represethe logic states 0 and 1.To perform logic funtion invertor and majority gate are needed. In QCA logic values are stored based on electron's charge rather than electrical pulse like in CMOS. The automatic logic synthesis for QCA circuits has the different aspects. The functional level:It is used to describing and generating a connectivity of the circuit to be realized. The physical level:It is used to describing and evaluating the cost a circuit interms of area,delay and energy dissipation. The geometric level:It is used to describing and generating the layout out QCA circuit.

III.BASIC QCA ELEMENTS

A.QCA Wire

The binary signal propagates from input to output because of the electrostatic interaction between cells. Moreover in a QCA wire, all the computational power is provided by the coulomb interaction between cells and there is no electrical current flow between cells and hence no power dissipation.

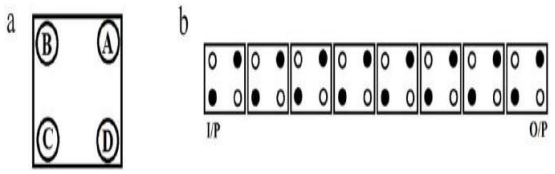

Fig.2 QCA Wire

B.QCA Wire-Crossing

In QCA, two kinds of QCA wire-crossing are possible-coplanar and multilayer. Coplanar wire crossing in QCA requires cells of two different orientations, a 90 degree and a 45 degree structure whereas multilayer wire crossing has no such strict orientations constrain. The crosstalk between the coplanar crossing can be avoided by introducing multilayer wire crossing.

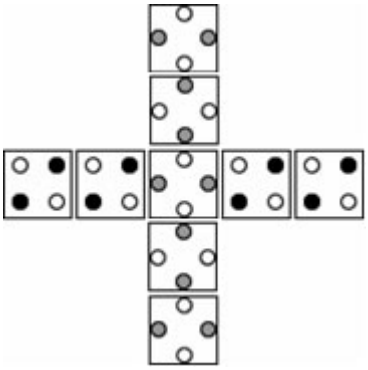

Fig.3. QCA Wire Crossing

C.QCA Majority Gate

The governing equation for the majority gate is, M(a,b,c) = ab+bc+ca. Two input AND and OR gates can be implemented with three input majority gates by setting one input to a constant with ANDs, ORs and Inverters, any logic function can be realized.

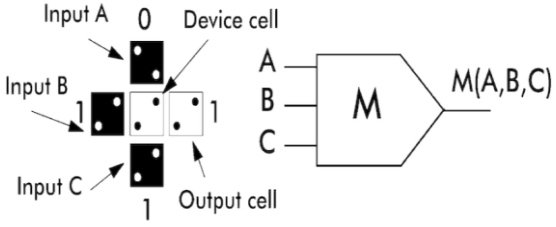

Fig.4.QCA Majority Gate

TABLE I. Truth table of majority gate

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

D.QCA Inverter

Two standard cells in a diagonal orientation are geometrically similar to two rotated cells in a horizontal orientation. For this reason, standard cells in a diagonal orientation tend to align in opposite polarization directions as in the inverter chain. The signal comes in from the left, splits into two parallel wires and is inverted at the point of convergence. An inverter gate can be implemented using 11 new proposed QCA cells.

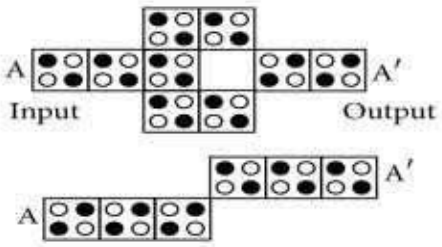

Fig.5. QCA Inverter

E.QCA Clocks

The circuit area is divided into four sections and they are driven by four phase clock signals. As shown in fig. 6, there is a 90 degree phase shift from one section to the next. In each clock zone, the clock signal has four states: high-to-low,low-to-high and high. The cell begins computing during the high-to-low state and holds the value during the low state. When the clock is in the low-to-high state, the cell become released and inactive during the high state.

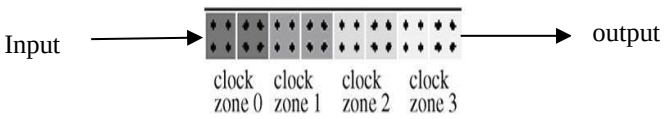

Fig.6.QCA Clock

The QCA clocking signal is used to control the signal propagation along the QCA cells arrangement. Then it is also used to synchronize the digital circuits. There are four-different clocking phases such as, SWITCH, HOLD, RELEASE and RELAX as shown in Fig.7.

SWITCH: During this phase, the inter-dot barriers are slowly raised and the computation takes place according to QCA cell arrangement.

HOLD: In this phase, the inter-dot barriers are kept high and the QCA cells retain their states.

RELEASE: The barriers are lowered and the cells are allowed to relax to unpolarized states during release phase.

RELAX: In this phase, the barriers are kept low and the cells remain in unpolarized state.

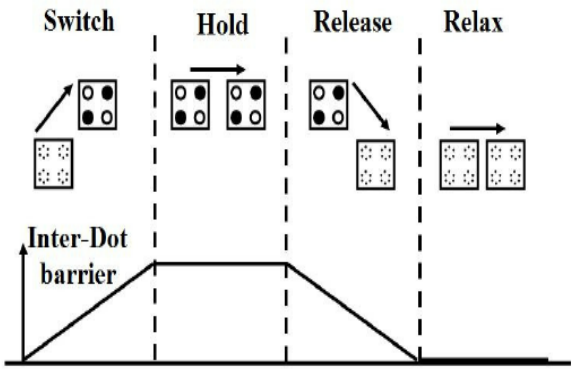

Fig.7.Four phases of clocking

IV.CELL MINIMIZATION TECHNIQUE:

The proposed design based on cell minimization technique used for reducing the majority gate.

1. The number of majority gate is connected spontaneously without using extra cells.

2. To reduce the length of the circuit the majority gates are aligned in parallel manner.

3. Directly the output and polarization are fixed in majority gates instead of using extra cells.

V .PROPOSED DESIGN OF FLIP-FLOPS

Flip-flop is a one bit storage device and it is the sequential circuit, whose output is depend on the present input as well as past output. Then the types are given below

SR flip-flop,D flip-flop,JK flip-flop,T flip-flop.

A.QCA Based SR Flip-flop Design

The SR flip-flop has two data inputs S and R. The S input is made high to store 1 in the flip-flop and R input is made high to store 0 in the flip-flop. In this when inputs are same then the output either does not change or it is invalid which is shown in Table 2.

TABLE II. Characteristic table of SR flip-flop

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	Intermediate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Intermediate

Characteristic equation of SR flip-flop:

$$Q(t+1)=S+R'Q$$

As shown in Fig. 8, the majority gate implementation of SR flip-flop has 1 majority gates and 3 inverters. In this S input is complement with the R input. The outcome of M1 is complemented and feedback to the S input .The output obtained by M1 is complemented to produce output Q0.

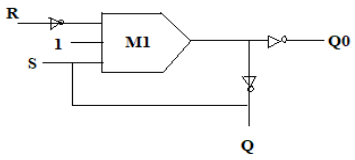

Fig.8 SR Flip flop design using Majority gate

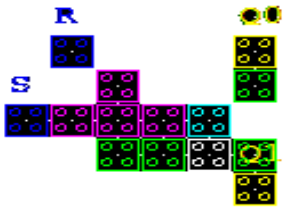

Fig.9 QCA cell layout of SR Flip flop

TABLE III.Performance Comparison of SR Flip Flop

S.No	Parameters	Existing system[1]	Proposed system
1	Complexity	38	14
2	Area	0.04μm^2	0.012 μm^2
3	Latency	1.5	1
4	Majority gate	4	1

B.QCA Based JK Flip-Flop Design

Inputs J and K behave like input S and R to set and clear the flip-flop(the letter J is for set and the letter K is for clear). When logic 1 input is applied to both J and K simultaneously, the flip-flop switches to its complement state, i.e., if Q=1, it switches to Q=0 and vice versa. The output Q is AND with K and clock pulse only if Q is previously 1.similarly, output Q' is AND with J and clock pulse only if Q was previously 1. The behavior of JK flip flop is demonstrated in the Table 4.

Characteristic Equation of JK Flip Flop: Q(t+1)=JQ'+K'Q

TABLE IV. Characteristic table of JK Flip Flop

Q	J	K	Qt+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

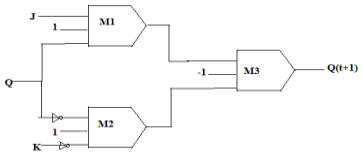

Fig.10 JK flip-flop design using majority gate

As shown in Fig.10 , the majority gate implementation of JK flip flop has 3 majority gates and 2 inverters. Input to M1 is J and Q, input to M2 is K' and Q' (complement of Q input given in M1). The output of M1 and M2 is given as a input to M3 which produces the output JQ'+K'Q.

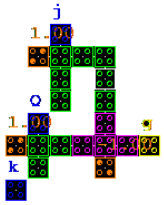

Fig.11 QCA cell layout of JK Flip-Flop

TABLE V. Performance Comparison

S.No	Parameters	Existing System[1]	Proposed System
1	Complexity	78	21
2	Area	0.071 μm^2	0.03 μm^2
3	Latency	1.5	1
4	Majority gate	6	3

C.QCA Based D Flip-Flop Design

The D flip flop is a modification of the clocked SR flip flop. It has two inputs: D and Clock. In D flip flop, the next state is always equal to the D input and it is independent of the present state. Therefore, D must be zero if Q t+1 have to be 0 and 1 if Q t+1 have to be 1,regardless of the value of Q which is shown in Table 6.

TABLE VI. Characteristic table of D Flip Flop

Q	D	Q t+1
0	0	0
0	1	1
1	0	0
1	1	1

Characteristic Equation of D Flip Flop: $Q_{(t+1)}=D$

Fig.12 D Flip Flop design using majority gate

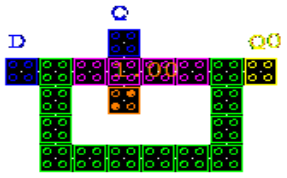

Fig.13 QCA Cell Layout of D-FF

As shown in Fig.12, the majority gate implementation of D flip flop has 1 majority gate. The input for M1 is D and Q . The output(Q0) is feedback to D to produce the result Q=D.

TABLE VI. Performance Comparison of D Flip Flop

S.No	Parameters	Existing System[1]	Proposed System
1	Complexity	43	20
2	Area	0.04 μm^2	0.02 μm^2
3	Latency	1.25	1
4	Majority gate	4	1

D.QCA Based T Flip-flop Design:

T flip-flop is also known as the Toggle flip-flop. The T flip-flop is a modification of JK flip-flop.

TABLE VII. Characteristic table of T Flip Flop

Q	T	Q (t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Table 7 shows that when T=1,the state of the flip-flop is complemented; when T=0,the state of the flip-flop remains unchanged. Therefore, for 0-0 and 1-1 transitions T must be zero and for 0-1 and 1-0 transitions T must be 1.

Characteristic Equation of T flip-flop Q(t+1)=TQ'+T'Q

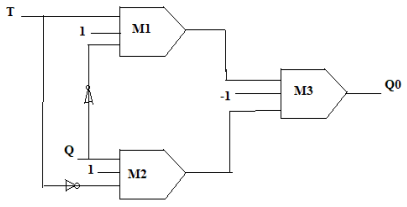

Fig.14 T Flip Flop design using majority gate

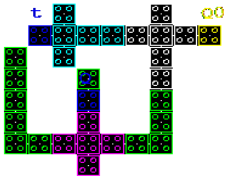

Fig.15 QCA cell layout of T Flip Flop

As shown in Fig.14, the majority gate implementation of T flip flop requires 3 majority gate. It is similar to that of JK flip flop. In T flip-flop, the input given to M1 is inverted and given as a input for M2. The outcome of M1 and M2 is given as a input to M3 which produces the result Q0=TQ'+T'Q.

VI. PROPOSED DESIGN OF COUNTERS

The Counters are designed by using group of Flip-Flops.Counter is similar to that of Shift Register in Construction.The only difference in this counter is the Feedback.It has two types one is Synchronous Counter another one is Asynchronous Counter.

A.QCA BASED RING COUNTER DESIGN

In this,4bit ring counter is designed which circulates 4bit data.The input data is given to the first Flip-Flop and clock pulse is given common to common to all the flip-flop and the clock pulse is applied for all the 4 flip-flops.On each successive clock pulse applied to the flip flops circulate between these four flip flops. For the proper circulating of data,the output of the fourth flip flop is feedback to the first flip flop i.e.,the output of the fourth flip flop is given as a input for first frlip flop.So that the data circulates repeatedly.

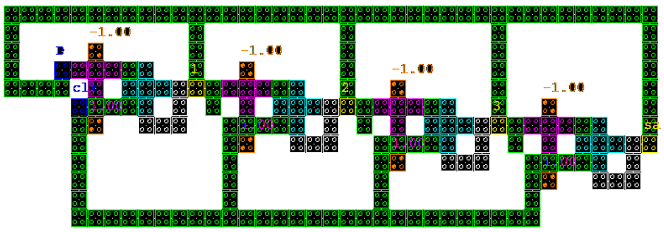

Fig 16. QCA cell layout of Ring Counter

The QCA Implementation of Ring Counter requires 201 cells,with an area of 0.18μm^2.By analyzing the concept of Ring counter,it was implemented in terms of QCA cell.In this we have designed Ring counter by the proposed design of D flip flop which are Optimized interms of area,complexity and latency.For Cell implementation of 4 bit Ring counter using D flip flop,it requires 4 D flip flop which is connected serially and the given as a common clock pulse.

TABLE VIII.Performance comparision of Ring Counter using D flip-flop**:**

S.No	**Parameters**	**Existing System [2]**	**Proposed System**
1	Cell count	342	201
2	Area	0.2μm^2	0.18μm^2
3	Latency	4	1.5
4	Majority gate	12	12

B.QCA BASED JOHNSON COUNTER DESIGN

The Johnson counter is also called as the twisted Ring counter. Johnson counter is similar to that of the Ring counter.

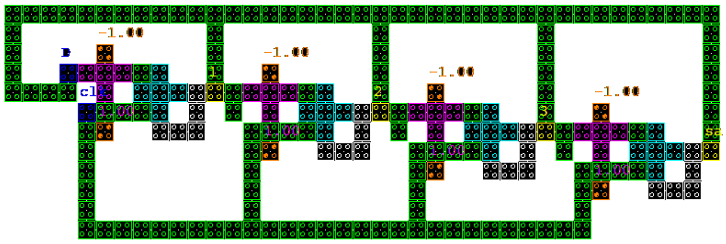

Fig 1.7.QCA cell layout of Johnson Counter

By analyzing the concept of Johnson counter,it was implemented interms of QCA cell.In this we have designed Johnson counter by the proposed design of D flip flop which are Optimized interms of area,complexity and latency.For cell implementation of 4 bit Johnson counter using D flip flop,it requires 4 D flip flop which is connected serially and the given as a common clock pulse.

TABLE IX. Performance comparision of Johnson counter using D flip-flop

S.No	Parameters	Existing System[22]	Proposed System
1	Cell count	232	208
2	Area	0.24μm^2	0.2μm^2
3	Latency	5	4
4	Majority gate	14	12

VII.RESULTS AND DISCUSSION

A.Simulation parameters

The design implementation and simulation is achieved through QCADesigner 2.0.3. The bistable simulation is carried with 18X18 nm QCA cell.

B.Simulation Output of Sequential circuits

The simulation result of the proposed sequential circuit is shown in Fig 18-23 and the verified with its truth table.

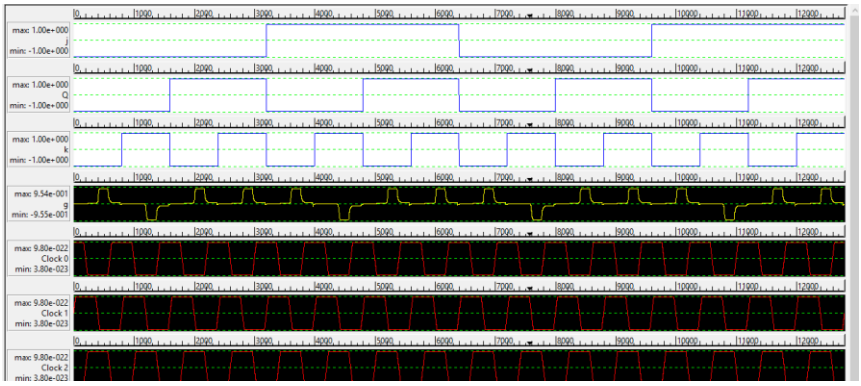

Fig.18 Simulation result of SR Flip-Flop.

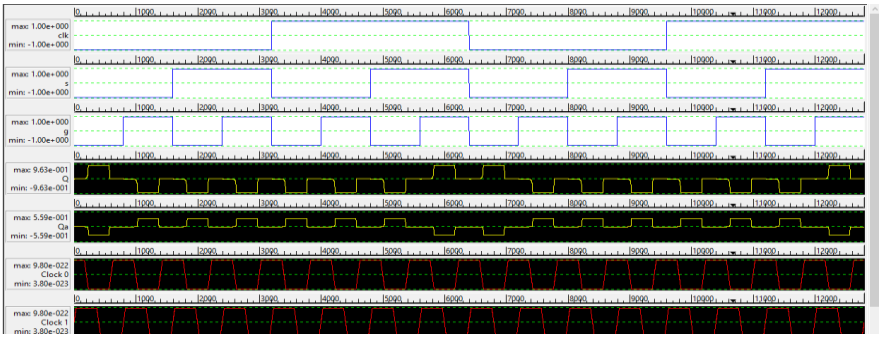

Fig. 19 Simulation result of JK Flip-Flop.

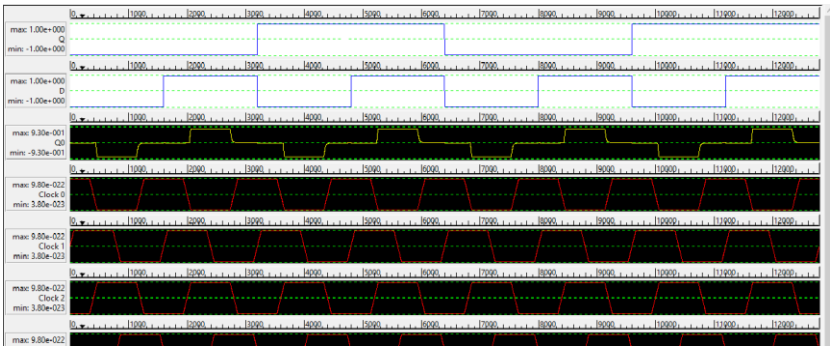

Fig.20 Simulation result of D Flip-Flop

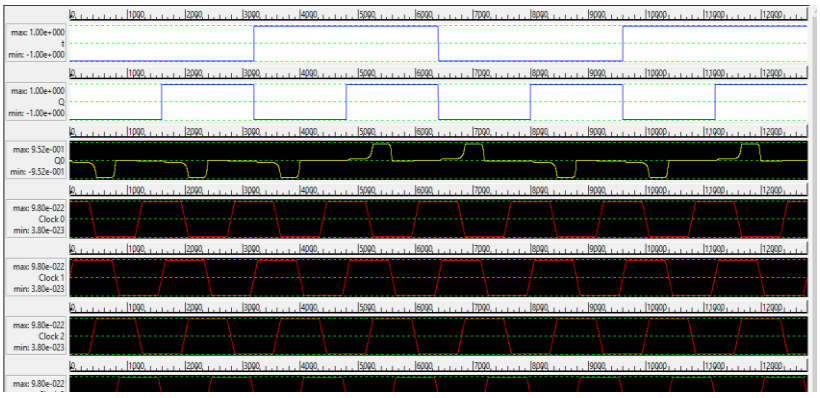

Fig. 21 Simulation result of T Flip-Flop

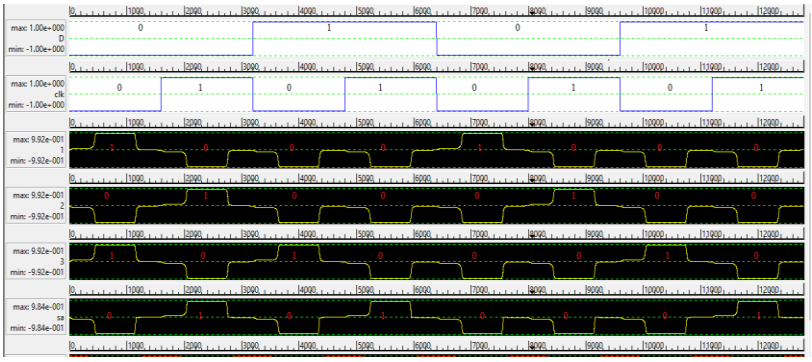

Fig. 22 Simulation result of Ring counter using D Flip-flop

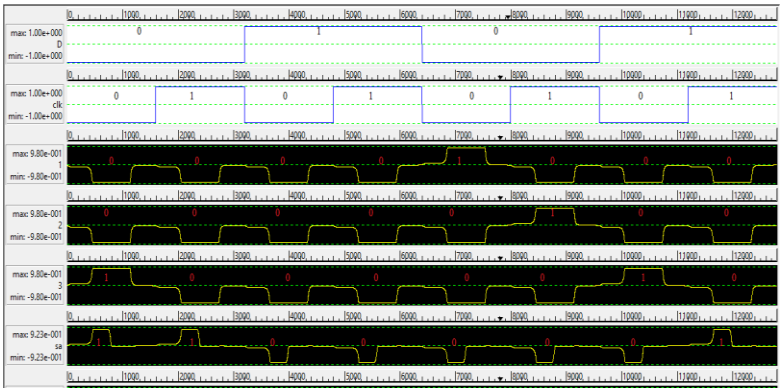

Fig.23 Simulation result of Johnson countert using D flip-flop

VII.CONCLUSION

In this paper, the optimized sequential circuits like flip-flops and Counters has been designed. The designed flip-flops with less complexity that has been used for the design of Counters. The QCA layout designs have minimum cell count and area leading to optimum design . The functionality of the different flip-flops, Counters are verified using QCADesigner 2.0.3.

REFERENCES

[1] Ratna Chakrabarty, A Novel Design of Flip-Flop circuit using Quantum Dot Cellular Automata 978-1-5386-4649-6/18/$31.00,2018 IEEE

[2] Birinderjit Singh and Balwinder Singh(2018).Quantum Dot Cellular Automata(QCA) based 4-Bit Shift Register using efficient JK Flip Flop.Volume 118 no.19 2018,143-157

[3] Kianpour et al. A Novel Quantum-Dot Cellular Automata X-bit x 32 bit SRAM IEEE Transactions on Very Large scConcurrently Testable Latches for Molecular QCA"IEEE Transactions On Nanotechnology, VOL. 9, NO. 1, January 2010.ale Intergration system 827-836,2016.

[4]kianpour et al. A novel Quantum Dot cellular automata x-bit x 32-bit SRAM IEEE Transaction on very large scale integration sytem 827-836,2016.

[5]A.Rezaei(2016),"Design of optimized quantum dot cellular automata RS flip flops "

[6]J.C Das, De, Optimized design of flip-flops using Quatum dot cellular automata,Quant.Matter 5 (5) (Oct , 2016) 680-688

[7]Shaahin Angizi,Samira sayedsalehi,Arman Roohi,Nader Bagherzadeh,keivan Navi (2015),"Design and verification of new n-bit quantum dot synchronous counters using majority function based JK flip flops".

[8]Mostafa Sadeghi,Akbar Napiollahi(2015),"Modeling and evalution of optimal T-flip flop based on Quantum cellular automata using QCA Designer simulator

[9]Dallaki.H,Mehran.M,(2015),Novel subtractor design based Quantum Dot cellular Automata nanotechnology,Int .J.Nanosci

[10]S.Sarmadi,S.Azimi ,S.Shekhfaal, S.Angizi, Designing counter using inherent capability of Quantum-dot cellular automata loops,Int.J.Mod.Educ.Compuy.Sci.(9)(2015) 22.

[11]W.Liu,M. O'Nelli,E.E.Swartzlander, A first step towards cost function for quantum dot cellular automata designs, IEEE Transaction.Nanotechnol.13(3) (2014) 476-487

[12]CaioAraujo T. Campos, Abner L. Marciano, Omar P. VilelaNeto, Frank Sill Torres, "USE: A Universal, Scalable and Efficient clocking scheme for QCA", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Journal of Latex Class Files, Vol. 11, No. 4, December 2014

[13]Bhattacharya.S,Ghatak.K.P,Quantum cellular automata recent trends and applications.Nova science publishers ,Inc.,USA(2013)

[14] Tamal Sarkar(2013) "Design of D flip flop using nano technology based Quantum cellular automata".

[15]Xiao,L.R.,Chen,X.X., Ying ,S.Y.,2012.Design of Dual-edge triggered flip-flops based on quantum do cellular automata. J.Zhejiang Univ-sci. C(comput. & Electron.),(5):385-392

[16]Askari.M,M.Taghizadeh ,2011.Logic circuit design in nano scale using Quantum dot cellular automata,in proc.Europian journal of scientific research,pp:5162-526,ISSN 1450-216X vol.48 No.3(2011).

[17]Kong et al.Counter designs in Quantum-dot cellular automata.10th IEEE Conference on NANO,2010.

[18]Karthigai Lakshmi.S,and Athisha.G (2010) Efficient design of logical structures and functions used nanotechnology based Quantum dot cellular automata design.*International journal of computer Applications(0975-8887),3,35.*

[19] [6]M.A. Amiri, M. Mahdavi, S. Mirzakuchaki, "QCA Implementation of a MUX-Based FPGA CLB", ICONN 2008, pp. 141–144.186 [7]Himanshu Thapliyal, Student Member, IEEE, and Nagarajan Ranganathan, Fellow, IEEE, "Reversible Logic-Based

[20]V.Vankamamidi, M. ottavi, F.Lombardi, Two dimensional scheme for clocking/timing of QCA circuits, IEEE Trans. Comput. Aided Des.Inegerated circ.syst.27(1) (2008)34-44

[21] T. Mohammad, "A New Architecture for T Flip Flop using Quantum Dot Cellular Automata", IEEE, 2011.

[22].J. Huang, M. Momenzadeh, F. Lombardi, "Design of sequential circuits by quantum-dot cellular automata", Microelectronics Journals. 38, 525–537, 2007.

[23]P.D. Tougaw and C.S. Lent, "Logical devices implemented using quantum cellular automata," Journal of Applied Physics, 75:1818, 1994. [3]C. S. Lent and B. Isaksen, "Clocked molecular quantum-dot cellular automata," IEEE Trans. on Electron Dev., 50(9): 1890– 1895, September 2003.